In The Claims:

Claim 1. (currently amended) A method of testing a chip that comprises an intellectual product circuit module, the method comprising:

providing a test pattern;

sequentially configuring a plurality of registers with the test pattern in a plurality of different states according to the test pattern; and

after all of the registers are configured with the test pattern, providing a test activating signal to the intellectual product circuit module in a next state, so that the intellectual product circuit module operates according to the test pattern from the registers.

Claim 2. (currently amended) A circuit for testing a chip that comprises an intellectual product circuit module, the circuit for testing the chip comprising:

a plurality of registers, coupled to the intellectual product circuit module to output signals stored in the registers to the intellectual product circuit module; and

a multiplexing ~~mutiplexing~~ finite state machine controller, coupled to the intellectual product circuit module and the registers, wherein

the multiplexing ~~mutiplexing~~ finite state machine controller receives a test pattern and sequentially configures the registers with the test pattern in a

plurality of different states, after all of the registers are configured with the test pattern, in a ~~the~~ next state the multiplexing ~~mutiplexing~~ finite state machine controller further provides a ~~the~~ test activating signal to the intellectual product circuit module so that the intellectual product circuit module is operated and tested according to outputs of the registers.

Claim 3. (original) The circuit according to claim 2, wherein the intellectual product circuit module further comprises a plurality of ports coupled to the registers.

Claim 4. (original) The circuit according to claim 2, wherein the test activating signal includes a synchronous clock signal.

Claim 5. (currently amended) The circuit according to claim 2, wherein each of the registers further comprises an enable input terminal coupled to the mutiplexing finite state controller capable of controlling the registers and asserting an enable signal to enable the registers to buffer the test pattern.

Claim 6. (currently amended) A circuit for testing a chip that comprises a plurality of intellectual product circuit modules, the circuit comprising:

a multiplexer controller, coupled to the intellectual product circuit modules to selectively output a test result from the intellectual product circuit modules;

a plurality of registers, coupled to the intellectual product circuit modules to output signals stored in the registers to the intellectual product circuit modules; and

a multiplexing ~~mutiplexing~~ finite state machine controller, coupled to the intellectual product circuit modules, the multiplexer controller and the registers, the multiplexing ~~mutiplexing~~ finite state machine controller receiving a test pattern to sequentially configure the registers with the test pattern in a plurality of different states, and after all of the registers are configured with the test pattern, providing a test activating signal to one of the intellectual product circuit modules in a next state, so that the intellectual product circuit module is operated according to the output of the registers, and the multiplexing ~~mutiplexing~~ finite state machine controller further controlling the multiplexer controller to selectively output the test results.

Claim 7. (original) The circuit according to claim 6, wherein each of the intellectual product circuit modules comprises a plurality of ports coupled to the registers.

Claim 8. (currently amended) The circuit according to claim 6, wherein the multiplexer controller further comprises a select input terminal coupled to the multiplexing ~~mutiplexing~~ finite state machine controller, so that the

multiplexing ~~mutiplexing~~ finite state machine controller controls the multiplexer controller to selectively output the test result.

Claim 9. (original) The circuit according to claim 6, wherein the test activating signal comprises a synchronous clock signal.

Claim 10. (currently amended) The circuit according to claim 6, wherein each of the registers further comprises an enable input terminal coupled to the multiplexing ~~mutiplexing~~ finite state machine controller, which respectively controls and enables the registers to buffer the test pattern.

Claim 11. (original) The circuit according to claim 6, wherein the chip is a system on chip.